CLAIM LISTING

1. (Previously Presented) A method of verifying a state of an element comprising:

determining if the state of the element is equal to an expected state using a verify circuit, wherein the state of the element is a state of the electrical resistance of the element; and

outputting a valid signal if the state of the element is equal to said expected state, wherein the element comprises a thin oxide gated fuse having an oxide that is less than 2.5nm thick.

2. (Cancelled)

3. (Cancelled)

4. (Original) The method of claim 1, including sensing the state of the element.

5. (Original) The method of claim 1, including generating a high signal if the state of the element is equal to said expected state.

6. (Original) The method of claim 1, including generating a low signal if the state of the element is not equal to said expected state.

7. (Original) The method of claim 1, wherein determining the state of the element includes determining states of first and second thin oxide gated fuses.

8. (Original) The method of claim 1, wherein outputting a valid signal includes determining if the states of both first and second thin oxide gated fuses is equal to a first and second expected states.

9. (Previously Presented) A method for verifying a state of a memory device comprising:

comparing a state of a first thin oxide gated fuse having an oxide that is less than 2.5 nm thick to a first expected state, and generating a first signal, wherein the state is a state of electrical resistance;

comparing a state of a second thin oxide gated fuse having an oxide that is less than 2.5nm thick to a second expected state, and generating a second signal, wherein the state is a state of electrical resistance; and

outputting a valid signal if both said first and second signals are the same.

10. (Original) The method of Claim 9, including outputting a valid signal if both said first and second signals are high.

11. (Cancelled)

12. (Cancelled)

13. (Original) The method of Claim 9, including determining if said state of said first thin oxide gated fuse is equal to said first expected state.

14. (Original) The method of Claim 9, including determining if said state of said second thin oxide gated fuse is equal to said second expected state.

15. (Original) The method of Claim 9, including mirroring reference and fuse currents.

16. (Original) The method of Claim 15, including comparing said reference and fuse currents.

17. (Previously Presented) A method for verifying a state of a thin oxide gated fuse memory device, comprising:

setting a first expected state;

sensing a state of a first thin oxide gated fuse having an oxide that is less than 2.5nm thick, wherein the state is a state of electrical resistance;

determining if said state of said first thin oxide gated fuse is equal to said first expected state and generating a first signal;

setting a second expected state;

sensing a state of a second thin oxide gated fuse having an oxide that is less than 2.5nm thick, wherein the state is a state of electrical resistance;

determining if said state of said second thin oxide gated fuse is equal to said second expected state and generating a second signal; and

generating a valid output if both said first and second signals are the same.

18. (Cancelled)

19. (Cancelled)

20. (Previously Presented) A memory device comprising:

at least one memory cell having at least one thin oxide gated fuse having an oxide that is less than 2.5nm thick;

at least one reference cell;

at least one verify circuit connected to said memory cell and said reference cell sensing a state of said at least one thin oxide gated fuse, wherein the state is a state of electrical resistance;

at least one exclusive nor gate connected to said verify circuit; and

a logic gate connected to said exclusive nor gate generating a valid signal.

21. (New) The method of claim 1, wherein the verify circuit comprises a current amplifier.